Standby working conditions of Apple notebook SMC (basic power-on (boot) process)

Introduction to SMC and BIOS of Apple Notebook Motherboard

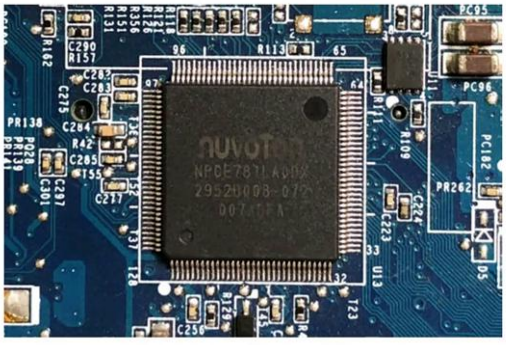
SMC :

Before getting to know SMC, we need to understand EC. EC (Embed Controller) is a 16-bit single-chip microcomputer. It also has a certain capacity of Flash inside to store EC code.Since the early EC mainly controlled the keyboard, it was also called KBC (KeyBoard Controller). The status of EC in the system is by no means inferior to the North-South Bridge, and controls the timing of most important signals when the system is turned on.

In the notebook, EC is always on, whether you are booting or shutting down, unless you completely remove the battery and adapter. In the shutdown state, the EC keeps running and is waiting for the user's startup information. After booting, EC acts as a keyboard controller, charging indicator, fan and other equipment control. It even controls the system's standby, hibernation and other states.

In Apple laptops, EC is named SMC (System Management Control) by Apple. Generally speaking, EC and SMC are the same chip, but in Apple laptops, SMC no longer manages the keyboard and touchpad. The difference in the manufacturer's design.

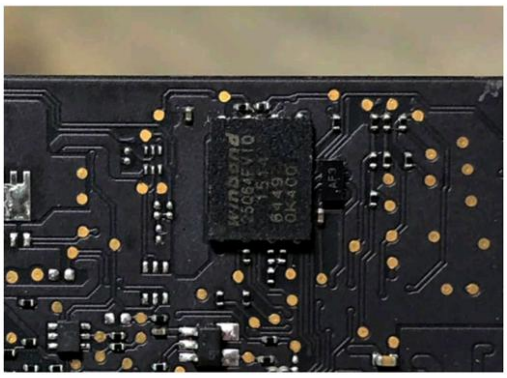
The picture below shows the comparison between Apple laptop SMC and EC material object from other manufacturers:

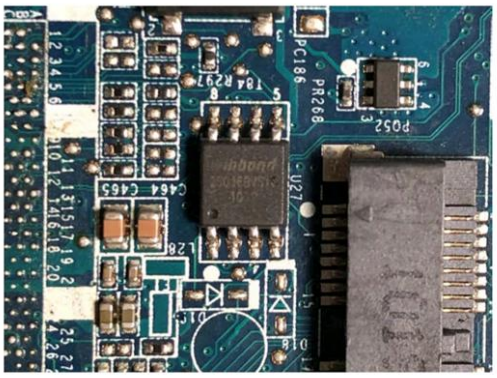


BIOS: BIOS is the abbreviation of "Basic Input Output System". In fact, it is a set of programs that are solidified on a ROM chip on the motherboard of the computer. It stores the most important basic input and output programs of the computer and self-check programs after booting. And the system self-starting program, it can read and write the specific information of the system settings from CMOS. Its main function is to provide the most basic and direct hardware settings and control for the computer.

Originally, BIOS refers to the program solidified on a ROM chip on the motherboard, but in actual repairs, we generally call this ROM chip a BIOS chip.

The following picture shows the comparison between the BIOS chip of Apple's notebook computer and the material object of other manufacturers' BIOS chips:





SMC's functions and working conditions:

The role of SMC: control the power on of the motherboard, control the temperature control and fan, control the backlight, manage the charging, etc.

SMC working conditions:

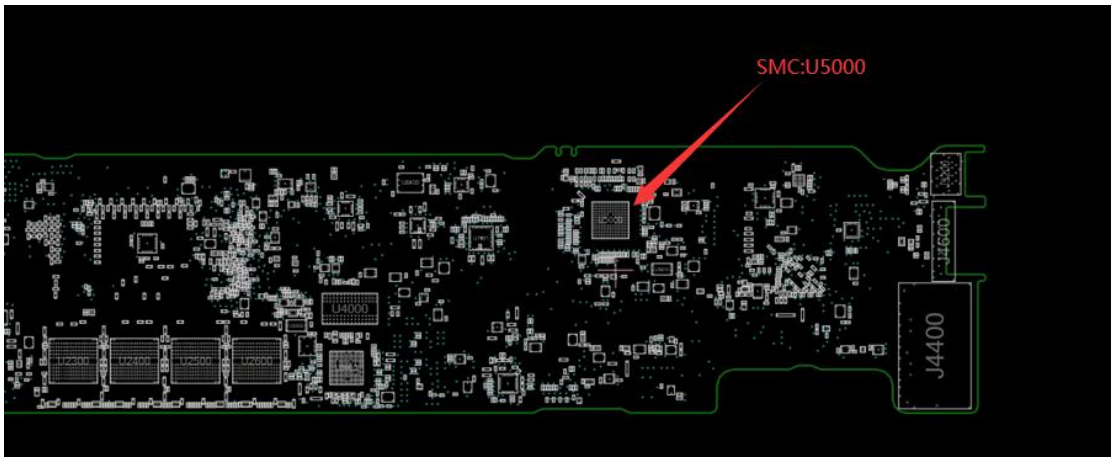
a. Standby power supply: In Apple notebook motherboards, the power supply names are generally VDD, VDDA, VDDC, VREF, etc., which are generally provided by PP3V42_G3H.

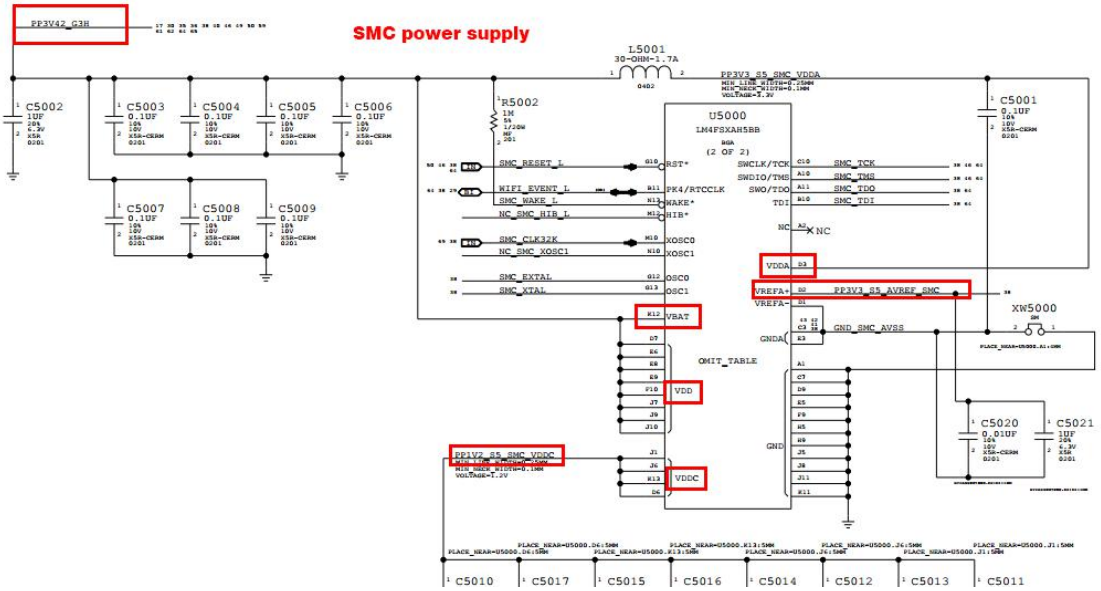
b. Standby clock: The clock name is generally SMC_XTAL, SMC_EXTAL. In Apple notebook motherboards, the SMC clock is generally 12MHz.

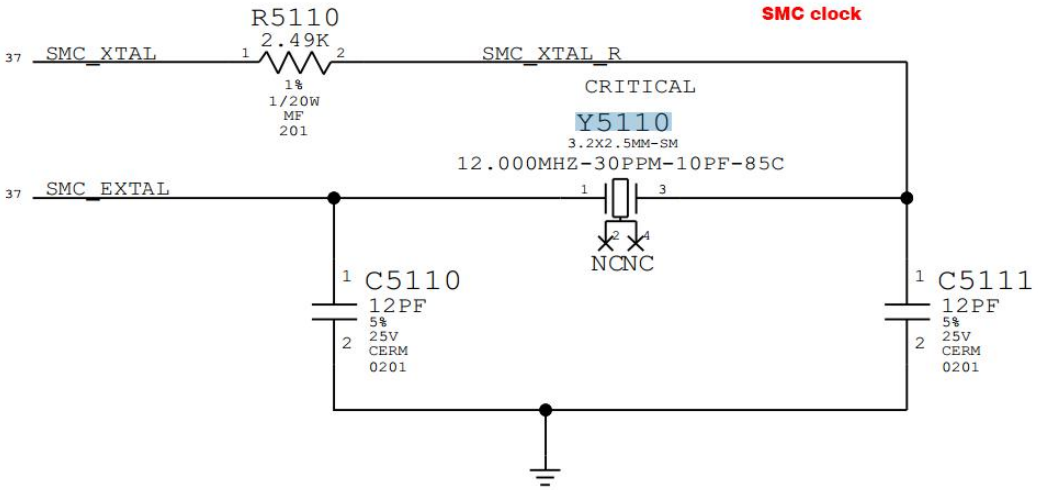
c. Standby reset: The reset name is generally SMC_RESET_ L, which is 3.3V.

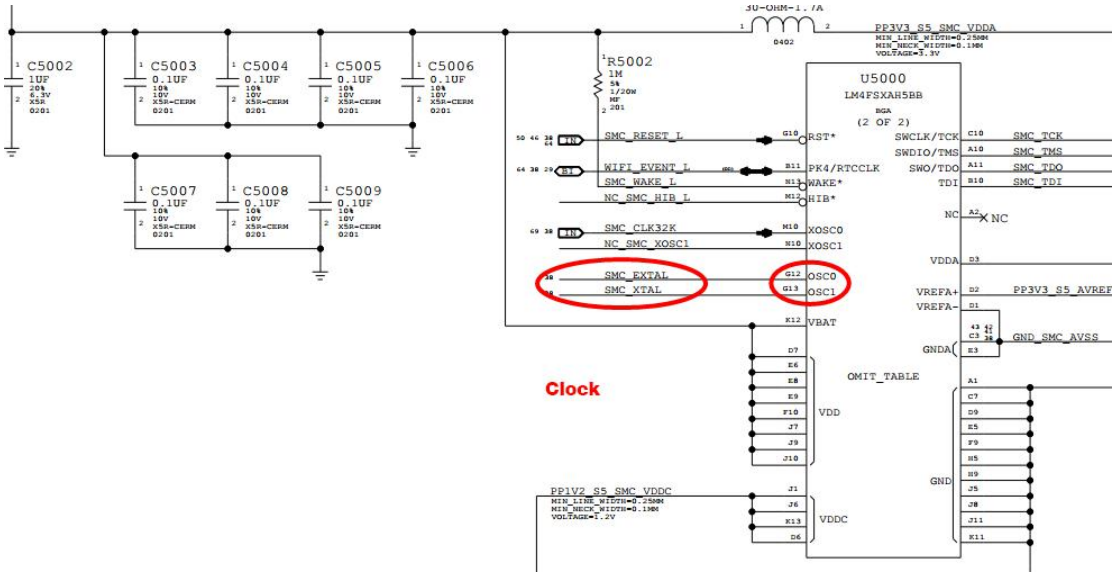
d. Program: Since most of the pins in the SMC are GPIO pins, a program is required to configure the pins. In the Apple notebook motherboard, the SMC has its own program.

Take MacBook A1466 as an example (the model with the largest number from 2013 to 2017):

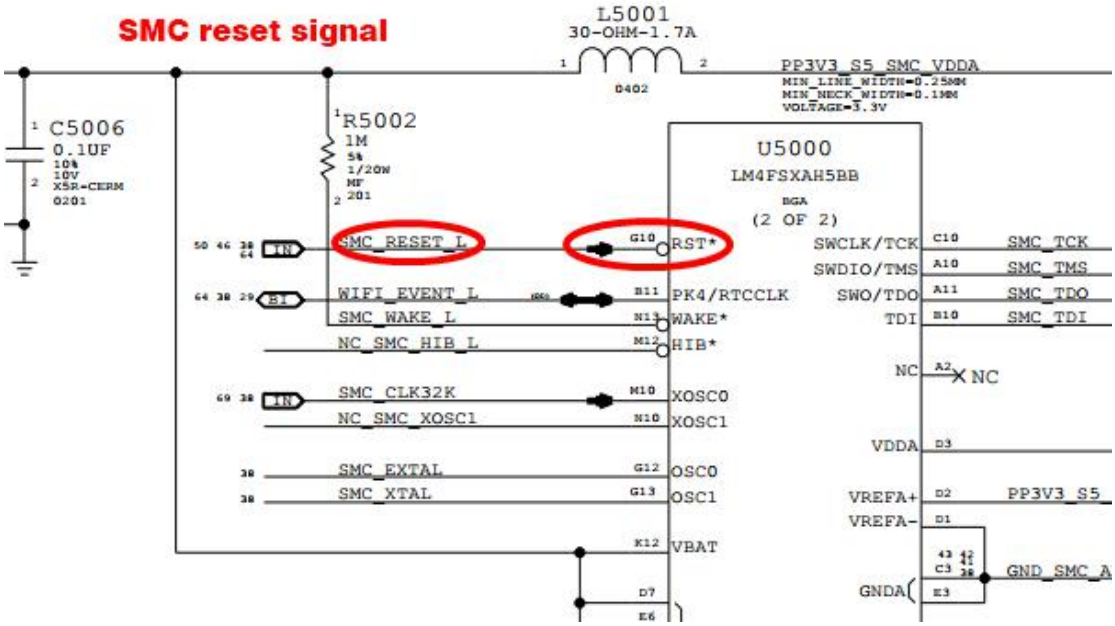




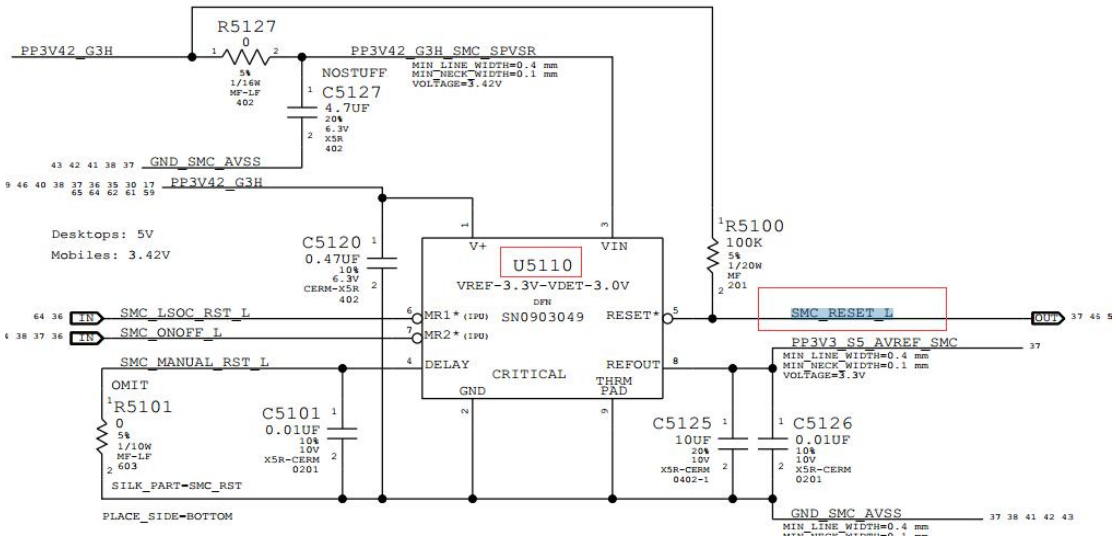




The clock signal is instantaneous, and it can only be detected when the SMC is powered on.



Search for reset signal in the schematic: SMC_RESET_L found to come from U5110



The reset signal voltage output by U5110 is 3.3V

Apple Notebook Motherboard-basic power-on (boot) process

Power-on process of Apple laptop:

In general, the laptop power-on process we are referring to refers to the process after pressing the power button until the screen appears. No matter what brand of laptop, the boot process is basically divided into hard start and soft start, hard start In the front, the soft start is in the back. Hard start refers to the power-on process of the motherboard, and soft start refers to self-checking and system related. The actual repair is mainly to repair the hard start. The following explanation mainly takes the Intel series chipset as an example.

The hard boot process of the notebook motherboard (take the Intel 4 series chipset as an example):

a. In the absence of any power equipment, the 3V button battery on the main board is used to generate VCCRTC and supply the RTC circuit of the South Bridge to keep the internal time running and CMOS information. After the South Bridge gets the VCCRTC, it will start the external 32.768KHz crystal oscillator, pull it up, and generate RTCRST# and SRTCRST# at the same time.
b. After plugging in the battery or adapter, the common point voltage is generated through the protective isolation circuit.
c. Then the standby chip generates the standby power supply of the EC, which is usually a linear voltage of 3.3V. After the EC is powered, it will let the external clock oscillation to obtain the standby clock, and after the EC reset, it will start to read the BIOS program to configure itself Foot position.
d. If the EC detects the power adapter, it will automatically send a signal to turn on the standby voltage of the South Bridge (VCCSUS3_ 3, V5REF_ SUS), and then send the RSMRST# signal to

notify the South Bridge that the standby voltage is normal at this time. If the EC cannot detect the adapter (battery mode)), the EC needs to receive the power-on trigger signal before turning on the standby power supply of the South Bridge to save power.

e. When the power button is pressed, a high-low-high (3.3-0-3.3V) startup trigger signal will be generated to the EC. After receiving this signal, the EC will send the PWRBTN# signal to the South Bridge.

f. After receiving the PWRBTN# signal, the South Bridge will send out SLP_ S5#, SLP_ S4#, SLP_ S3# signals in sequence. SLP_ S5/S4# (Via EC conversion) controls the generation (in S3 state) voltage and memory power supply, SLP_ S3# (Via EC conversion) controls the generation (in S0 state) voltage, such as VCCP (bus power supply), South Bridge Power supply, graphics card power supply, etc.

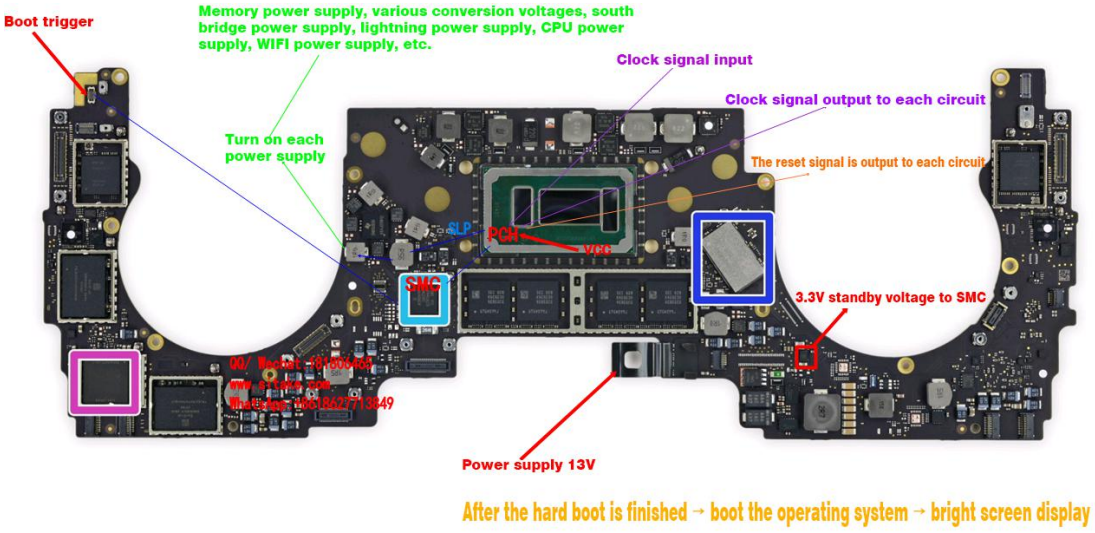
g. At the same time, after EC receives SLP_S3#, it delays 99ms to send VR_ON to the CPU power supply IC, and turn on the core voltage (VCORE) of the CPU. So far, the voltage of the whole machine has been turned on.

h. After the CPU power supply is normal, the CPU power supply chip sends VRMPWRGD to the South Bridge, and the South Bridge outputs various clocks to the outside.

i. After the South Bridge receives VRMPWRGD, S0Whole machine voltage power signal PWROK (usually issued by EC), it sends out CPUPWRGD to inform the CPU that its core voltage is complete and sends out PLTRST# and PCIRST# reset signals at the same time, where PLTRST# will go north bridge.

j. After the North Bridge receives PLTRST#, it sends out CPURST# to reset the CPU, and the CPU officially starts to work.

At this point, the hard boot is complete.



Based on the above, we can divide the power supply of the laptop into 4 levels:

G3 state voltage: the voltage generated when the adapter is just plugged in, generally refers to the common point voltage and the EC voltage (linear voltage)

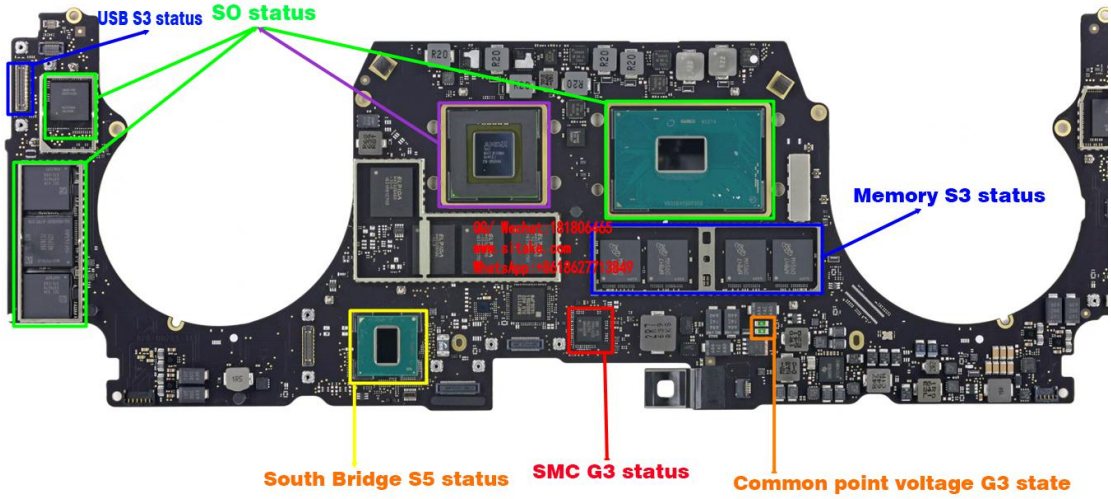
S5 state voltage: the voltage when the entire system is turned off (shutdown state), generally

refers to the 3V standby voltage of the South Bridge (generated by the standby chip).

Repair does not trigger, mainly repairs G3 and S5

S3 state voltage: the voltage in sleep state, generally refers to the voltage of USB and memory.

S0 state voltage: the voltage in the running state (boot), generally refers to the power supply of the south bridge, the power supply of the memory, the power supply of the graphics card, the power supply of the bus, the power supply of the CPU, etc.



Intel standard boot sequential explanation:

VCCRTC
RTCRST#
32.768KHZ
The above three sequential belong to the South Bridge PCH real-time clock module

VccSus3_3
RSMRST#
PWRBTN# (Press the power button)

SLP_S5#
SLP_S4#
SLP_S3#
The above three SLP signals, turn on each power supply of the motherboard

VDIMM
Vcc

VCORE
VRMPWRGD

CLK GEN
PWROK

CPUPWRGD
PLTRST#
PCIRST# CPURST#

VCCRTC: The power supply of the South Bridge RTC real-time clock circuit is 3V, which supplies power to the CMOS (RAM) module inside the South Bridge.

RTCRST#: The reset signal of the South Bridge RTC real-time clock circuit is 3V. After ICH9, an RTC reset signal has been added, named SRTCRST#.

32.768KHz: The clock signal of the South Bridge RTC real-time clock circuit. After the South Bridge gets VCCRTC and RTCRST#, it will give an external 32K crystal oscillation.

V5REF_ SUS: The 5V standby voltage of the South Bridge ACPI module (the new model no longer has this 5V)

VCCSUS3_3: 3.3V standby voltage of South Bridge ACPI module

VCCSUS1_05: The 1.05V power supply generated inside the South Bridge for itself (don't care about this voltage)

RSMRST#: The reset clear signal of the ACPI module inside the South Bridge informs the South Bridge that the 3.3V standby voltage is normal and the voltage is 3.3V. Controlled by an external circuit.

SUSCLK: The 32K clock sent by the South Bridge after RSMRST# is received. Most machines do not use it and can be ignored. New machines will be sent to EC for use.

PWRBTN#: Abbreviation of POWER BUTTON, power button trigger signal, 3.3V-0-3.3V pulse signal, falling edge trigger, generally sent by EC to South Bridge.

SLP_ S5#: The control signal for the South Bridge to exit the shutdown state.

SLP_ S4#: The control signal for the South Bridge to exit the dormancy state (Generally, only one of S5# and S4# is used to control the generation of memory power supply).
SLP_S3#: The control signal for the South Bridge to exit the sleep state (usually used to control the South Bridge power supply, bus power supply, independent display power supply, CPU power

supply, etc.).

VDIMM: refers to memory power supply

VCROE, VCC: Each S0 state power supply, such as CPU power supply, etc.

VRMPWRGD: The CPU power supply is good signal, notify the South Bridge, at this time the CPU power supply is normal.

CLK GEN: Clock turn-on signal, the clock chip works and outputs various clocks.

PWROK: S0complete machine voltage power supply is good signal, inform the South Bridge that the power supply is normal at this time.

CPUPWRGD: The PG signal sent by the South Bridge to the CPU is 1.05V to inform the CPU that its Core voltage is normal.

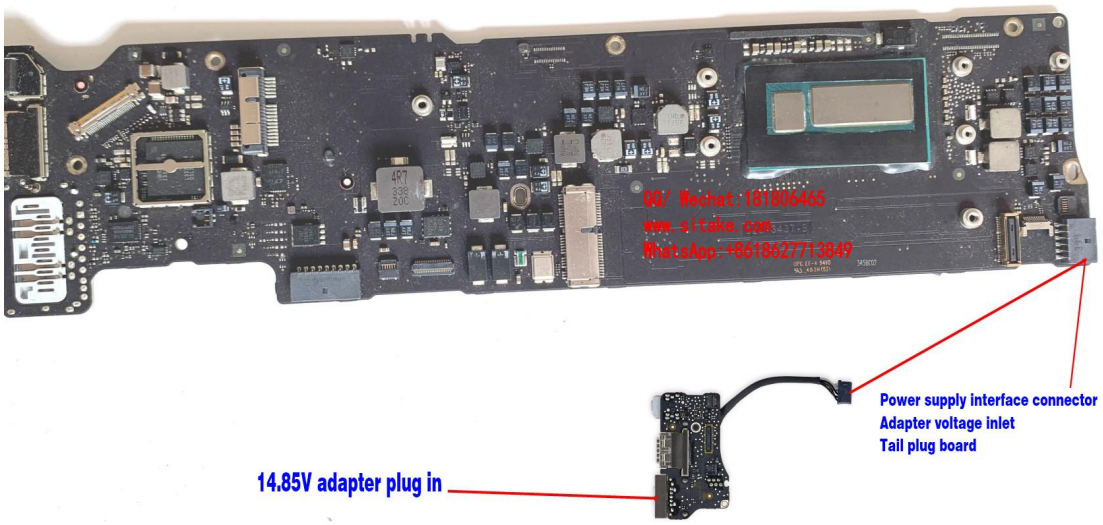
PLTRST#: Platform reset signal, the first reset issued by the South Bridge, mainly to the North Bridge, which is 3.3V.

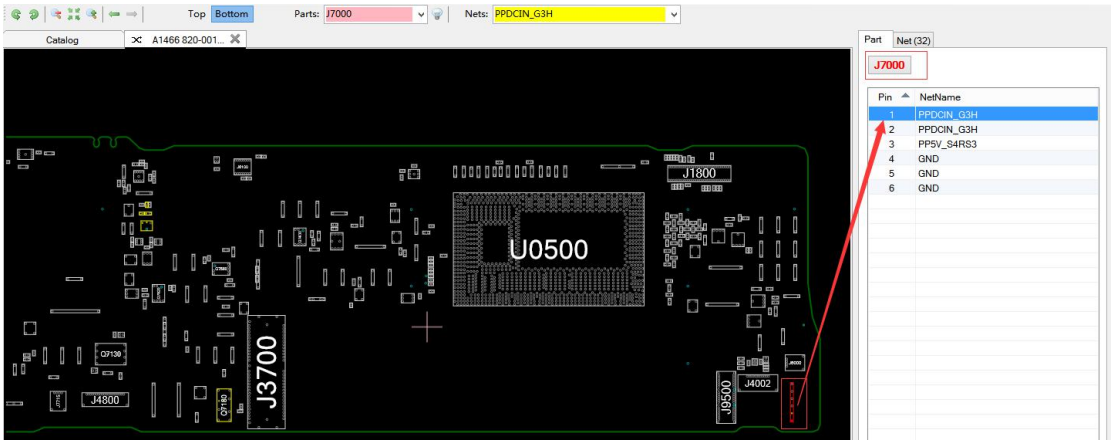
PCIRST#: PCI reset signal, the second reset issued by the South Bridge, usually for the MINI slot, network card, etc., is 3.3V.

CPURST#: The reset signal sent to the CPU by the North Bridge after receiving PLTRST# is used to reset the CPU. The voltage is 1.05V.

The above sequence and sequence are interpreted as hard-start sequence, which is also the main fault repair range. Soft start is the automatic boot of the software system under normal conditions.

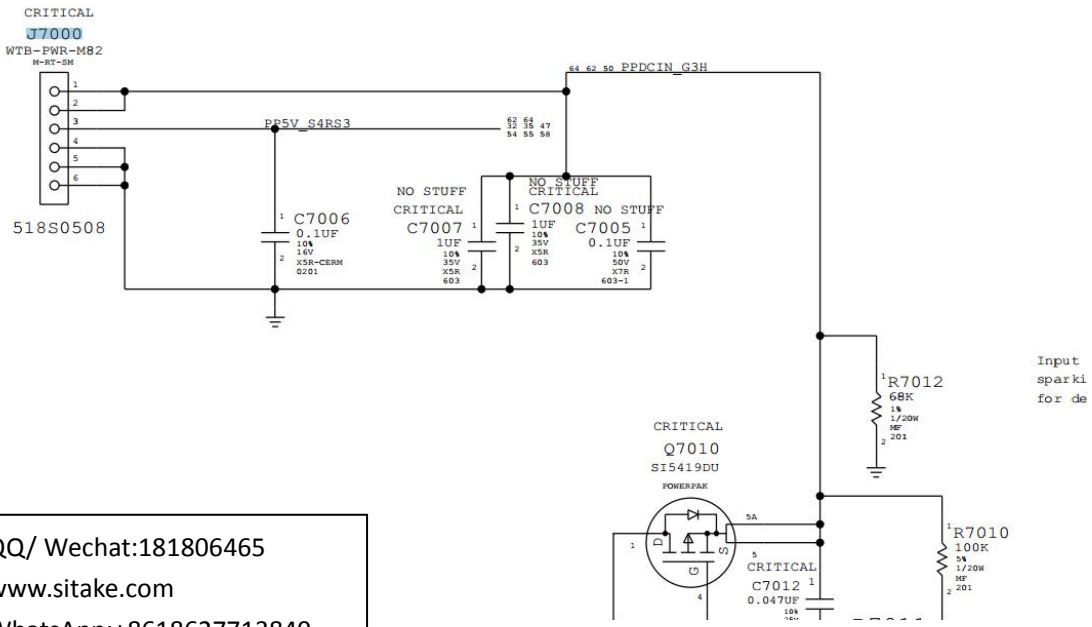
The hard boot is marked in the material object diagram, MacBook A1466 as an example (by knowing one method you will know all):

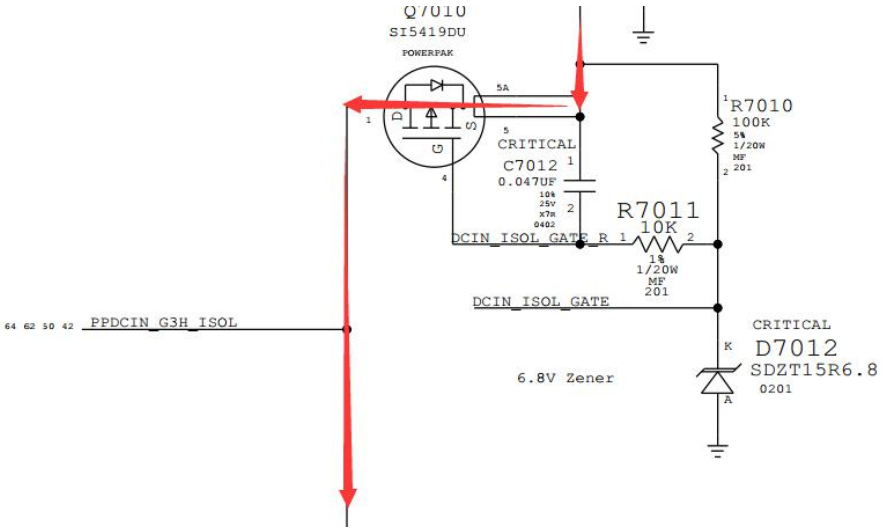




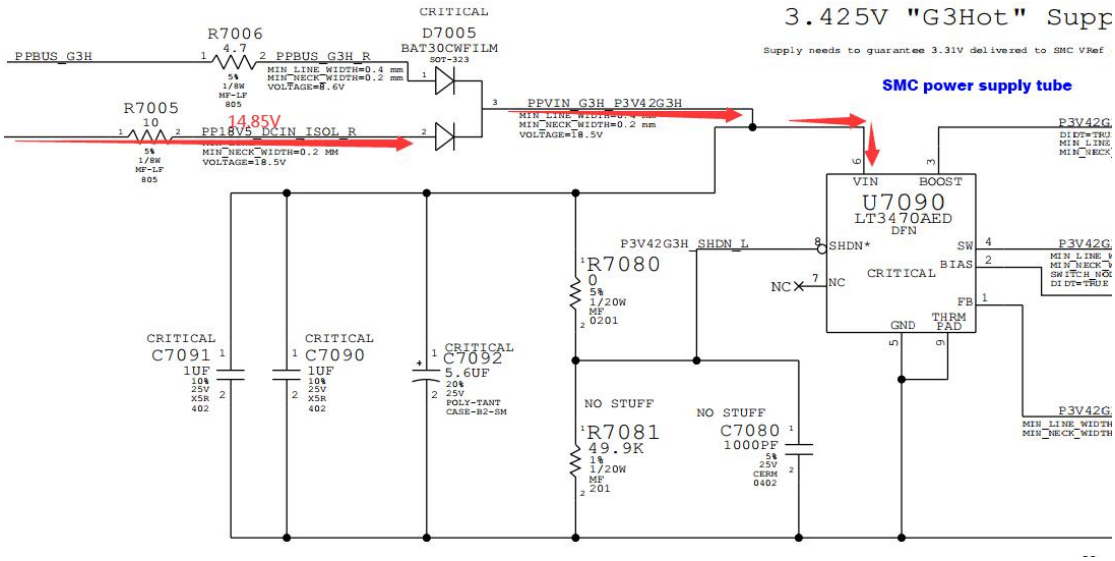
The material object motherboard compares the bitmap, and learns that the name of the battery interface in the circuit diagram is: J7000

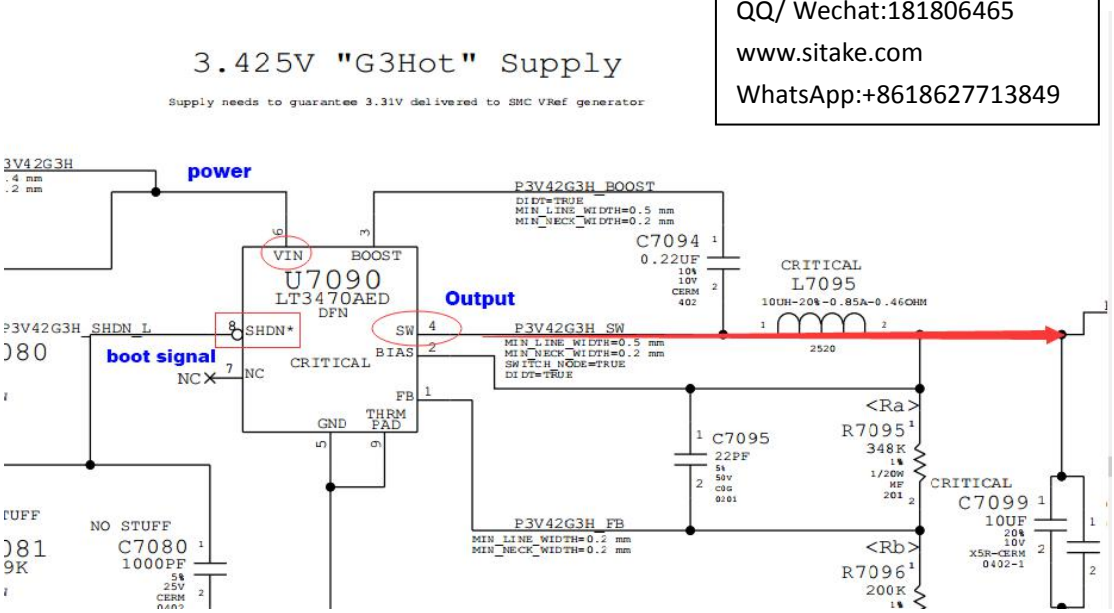
Then search for J7000 in the schematic



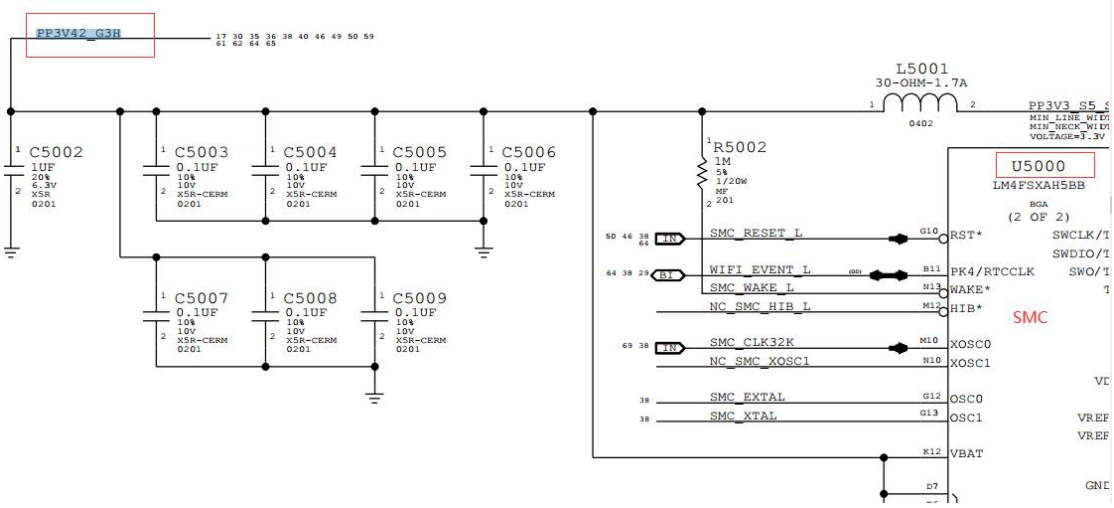


Q7010 low level conduction

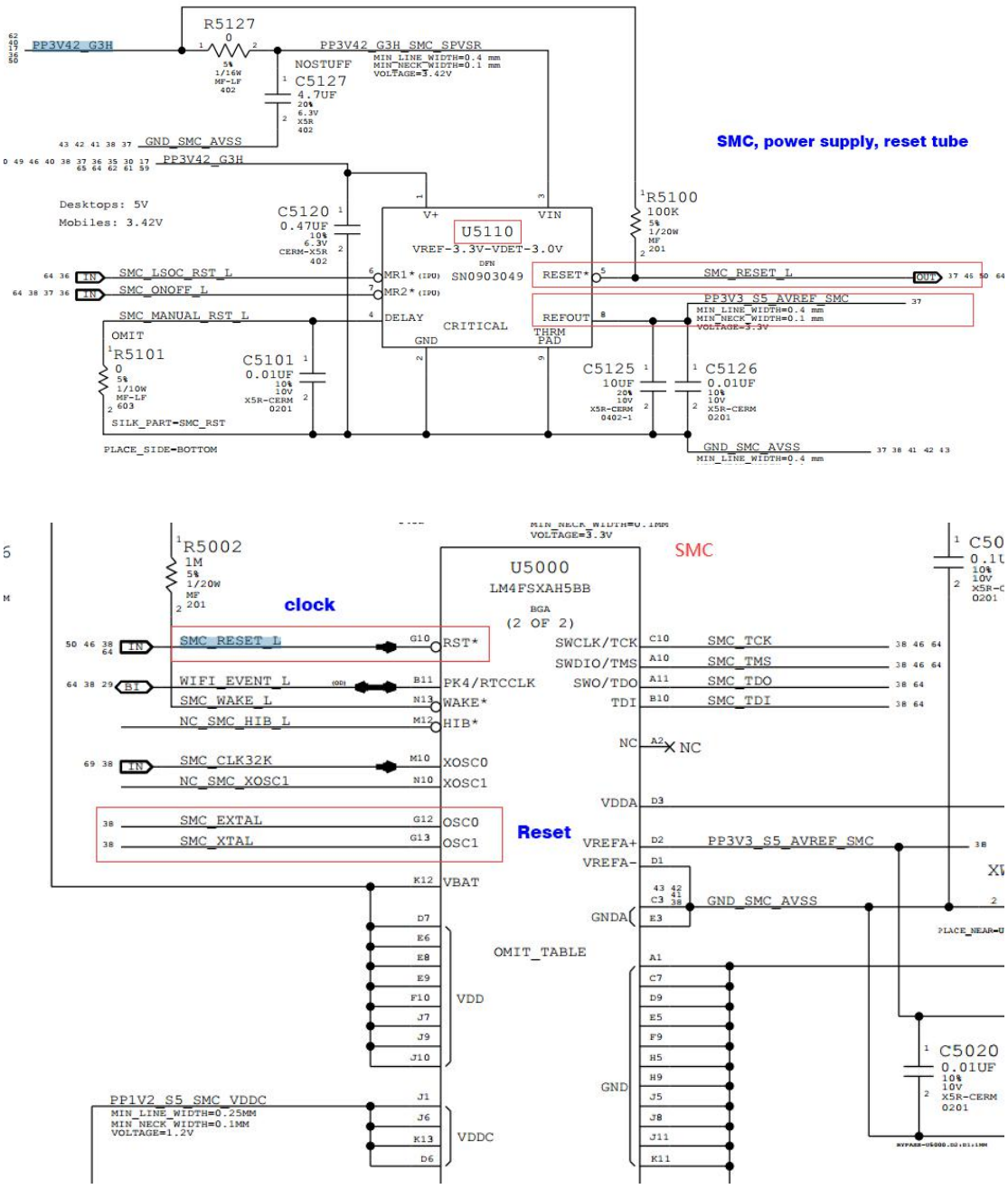




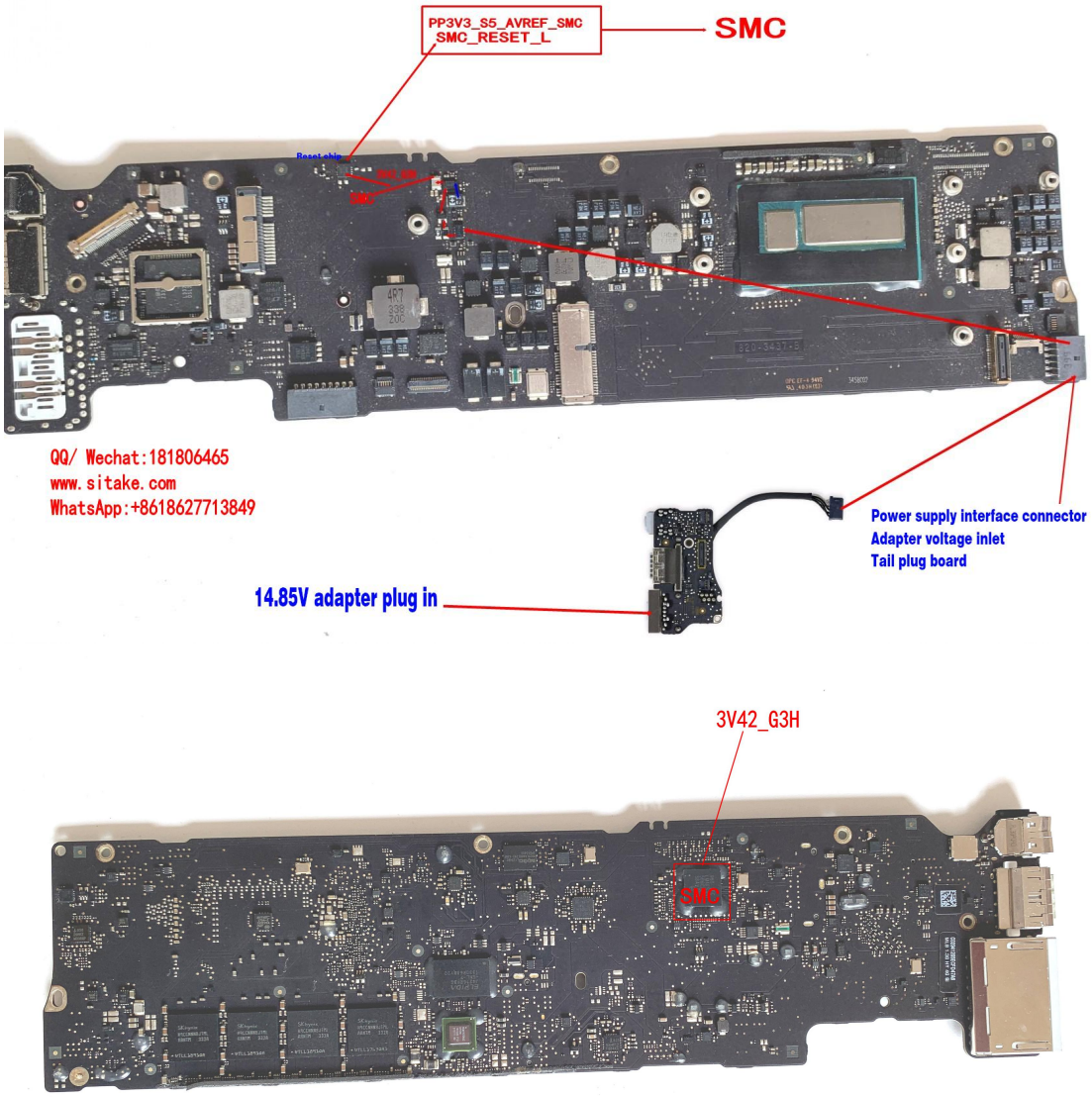
U7090 working conditions are normal, the feedback circuit is also normal, it will output: PP3V42_G3H, PP3V42_G3H to supply power to many circuits, but the most important thing is to supply power to the SMC:



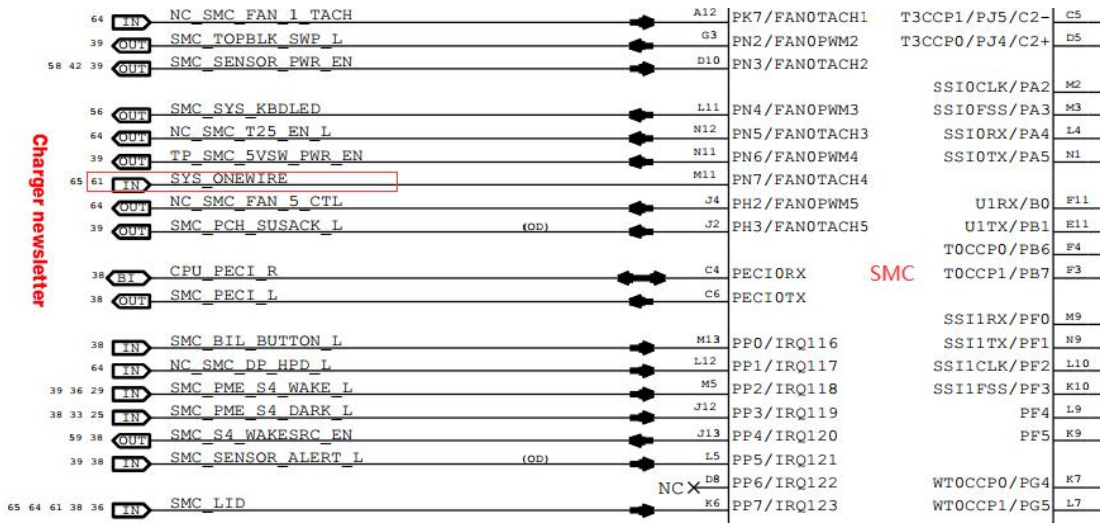
PP3V42_G3H is the earliest power supply generated on the motherboard (G3 state), at this time the common point voltage has not yet been generated.



After the SMC satisfies the power supply, reset, and clock, it reads the internal program, starts to configure the pin function, and turns on the South Bridge standby.



After the SMC works normally, it communicates with the charger through SYS_ONEWIRE, and the charger lights up in green (the single board turns green to yellow and orange if the battery is not inserted). You can judge whether the SMC is working normally by whether the green light is on.



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